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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,273	09/02/2005	Adrianus Marinus Gerardus Peeters	NL 020555	3515

24737 7590 08/28/2007

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	PAPER NUMBER
2117	

MAIL DATE	DELIVERY MODE
08/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/518,273	PEETERS, ADRIANUS MARINUS GERARDUS	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) ____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a non-Final Office Action in response to the Amendment filed 8/6/2007.

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) to (EPO) 02077495.6, filed 06/21/2002. The certified copy has been filed in parent Application No. 10/518,273, filed: 09/02/2005.

The present US Application is a 371 of PCT/IB03/02387, filed 06/05/2003.

Claims 1-7 are presently under examination and still pending in the Application.

Te objection to the drawings for proper functional description has been withdrawn in view of the Replacement Sheets of Figs. 1, 2 and 6, received on 8/6/2007, which are acceptable.

Objection to the specification has been withdrawn in view of the amendment to the abstract of the disclosure.

Objection to the Claims for element line indentations has been withdrawn in view of the amendment to the claims.

Rejection of the Claims under 35 U.S.C. 112, second paragraph, has been withdrawn in view of the amendment to the claims.

Response to Arguments

Applicant's arguments in the Amendment filed 8/6/2007, with respect to the rejection of claims 1-7 under 35 U.S.C. 102(e) as being anticipated by Chen et al. (US Patent No. 6,895,540), have been fully considered and are persuasive. Therefore, the rejection has been withdrawn in view of applicant's claim for foreign priority under 35

U.S.C. 119(a)-(d) to (EPO) 02077495.6, filed 06/21/2002, which predates the Chen reference filed on 8/18/2002.

However, upon further consideration, a new ground(s) of rejection is made, as set forth in the present Office Action, below.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "a delay element coupled to cause a relative delay between the times after which signals at the inputs affect the interface element", which renders the claims indefinite, because the expression "the times" fail to properly define relative delay between different time intervals or periods. Perhaps, a proper way to define is to change the "times" to "time intervals" as described in the abstract and recited in the method claim 7.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Narayanan et al. (US 6,081,913) issued, June 27, 2000.

Regarding independent Claims 1, 7, Narayanan discloses a scan design test circuitry and method, comprising:

Components (logic circuitry 501 associated with scan chain 107, Fig. 5) that operate asynchronously of one another.

An interface element (gating circuit 201, Figs. 2, 3, 5 and 7) having an output (103, 105) and at least two inputs (305, 307, Fig. 3) from the flip-flops (107N and 107N-1) each input coupled to a respective (flip-flop).

The gating circuit 201 supplying logic output signal (103, 105) that is a logical function of signals at the inputs (305, 307, Fig. 3), dependent on the relative timing due to (propagation delay) with respect to each other (305, 307) input.

A delay element (mutual exclusivity circuit 701) coupled to the gating circuit 201 via (local_sub_tri_en) signal, 203 causing a short propagation delay, which is a predetermined short delay from the second flip-flop 903, the inverter 905 and the

AND-gate 907, so that the duration of the local_rst_tri_en "pulse" is sufficient to allow the flip-flops of the scan chain 107 to properly store the response data, Figs. 7 and 10.

A conventional test access port (TAP) controller, which provides the rst_tri_en signal to the gating circuits, causes the delay element 701 to output the loca_rst_tri_en "pulse" 203, Figs. 7, 9 and 10.

Regarding Claims 2-3, Narayanan discloses when the delay_en signal is deasserted, at a logic low level, the mutual exclusivity circuit 1100 is configured in the normal scan test mode. The logic low level of the delay_en signal causes the multiplexer 1103 to output to the inverter 905 the Q2 signal received from the second flip-flop 903, which in effect bypasses the third flip-flop 1101 and operates as described in conjunction with Figs. 9 and 10.

In contrast, when the delay_en signal is asserted, the mutual exclusivity circuit 1100 is configured in the delay test mode. In the delay test mode, the rst_ tri_en signal is asserted for two clock cycles (instead of one as in the normal scan mode) to allow the circuit under test to receive two consecutive capture edges for this embodiment of the delay testing scheme.

Regarding Claim 4, Narayanan discloses FIG. 3 is a circuit diagram of a conventional gating circuit 201. In this example, the gating circuit 201 includes a two-input OR-gate 301 and a two-input AND-gate 303. The OR-gate 301 has an inverting input lead connected to receive the rst_tri_en signal. The other input lead of the OR-gate 301 is connected to the output lead 305 of the flip-flop 107N. The AND-gate 303 has one input lead connected to receive the rst_tri_en signal while its other input lead is connected to the output lead 307 of the flip-flop 107N-1. The rst_tri_en signal is

generated to have a logic high level during the normal functional mode and to have a logic low level during the scan mode.

Regarding Claims 5, 6, Narayanan discloses a conventional test access port (TAP) controller, which provides the rst_tri_en signal to the gating circuits causes the delay element 701 to output the loca_rst_tri_en "pulse" 203, Figs. 7, 9 and 10.

A scan chain 107, which is serially loaded with test patterns to test the circuit 100 using well known scan design techniques. The test patterns are typically generated using an automatic test pattern generation (ATPG) software tool, which are well known in the art of test circuits, Fig. 7.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis-Jacques can be reached on (571) 272-4150. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JAMES C KERVEROS
Primary Examiner
Art Unit 2117

Date: 17 August 2007
Office Action: Non-Final Rejection

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